

REMARKS

Claims 1-20 are pending in the present application. Claims 1, 18, and 19 are independent claims.

Allowable Subject Matter

Applicants acknowledge the Examiner's indication that claims 5-8 and 13-16 are allowed.

Rejection Under 35 U.S.C. § 102

In the present Office Action, the Examiner indicates that claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,541,926 to Saito et al. (hereafter "Saito").

The Examiner further makes the general statement that "original claims 1-4, 9-12, and 17-19 remain rejected" (page 2). Since the Examiner does not explicitly state the grounds of rejection for these claims in the present Office Action, Applicants must presume that claims 1-4, 9-12, and 17-19 are also rejected under § 102(b) as being anticipated by Saito.

Independent claims 1, 18, and 19 recite that data is distributed to a plurality of time slots to be sent to an STM circuit interface. These claims further recite providing a buffer for each of the plurality of time slots. In the Reply filed April 6, 2005, Applicants argued that Saito failed to teach these features.

However, in response to Applicants' arguments, the Examiner asserts that Saito "essentially teaches" that a buffer is provided in each time slot, citing Figs. 17, 20, and 21 and col. 18, lines 10-13.

Respectfully, Applicants wish to point out that the Examiner is applying the wrong standard for determining anticipation under § 102. Section 2131 of the MPEP sets forth the correct standard to be applied under § 102:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. Of California*, 814 F2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The **identical invention must be shown in as complete detail as is contained in the ... claims.**" *Richardson v. Suzuki Motor Co.*, 868 F2d 1226, 1236, 9 USQP2d 1913, 1920 (Fed. Cir. 1989)."

(emphasis added). Thus, § 102 is satisfied only by the reference showing every claimed feature **in as complete detail** as the claims, not by "essentially teaching" the features.

Furthermore, Applicants respectfully disagree with the Examiner that the cited portions of Saito even provide an "essential teaching" or suggestion of a buffer for each time slot. Fig. 17 clearly shows a single jitter absorption buffer unit 612 (also, see col. 20, lines 5-45). Furthermore, nothing in Figs. 20 and 21, or in col. 28, lines 10-13, discloses the use of more than one jitter absorption buffer unit. As independent claims 1, 18, and 19 clearly require a buffer provided in **each of a plurality** of time slots, Applicants submit that Saito fails to disclose every feature of the claimed invention.

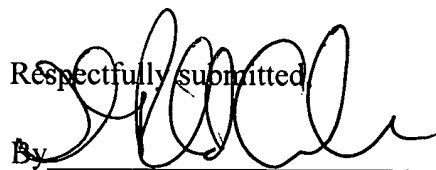
Furthermore, Applicants point out that Saito expressly teaches that, "when the STM frame mode is selected at the output processing unit 603 side, the data can be loaded into any desired time slot from the buffer unit 602." According to this disclosure in Saito, the data is first accumulated in the buffer unit 602, and **then** the accumulated data is dispersed therefrom into the plurality of time slots. Accordingly, Saito directly **teaches away** from each of the time slots being provided with a buffer, as required by the claims.

At least for the reasons set forth above, Applicants respectfully submit that independent claims 1, 18, and 19 are allowable. Furthermore, it is respectfully submitted that claims 2-4, 9-12, 17 and 20 are allowable at least by virtue of their dependency on claim 1. Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Conclusion

Entry of this Request for Reconsideration is respectfully requested. In view of the above remarks, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,


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